29.9 A Single-Inductor Switching DC-DC Converter with 5 Outputs and Ordered Power-Distributive Control

Hanh-Phuc Le[1], Chang-Seok Chae[1], Kwang-Chan Lee[1], Gyu-Hyeong Cho[1], Se-Won Wang[2], Gyu-Ha Cho[3], Sung-il Kim[4]

[1]KAIST, Daejeon, Korea, [2]Korea Electronics Corporation, Seoul, Korea
[3]JDA Technology, Daejeon, Korea, [4]LG-PERI, Kyunggi-do, Korea

Single-inductor multiple-output (SIMO) switching converters can support more than one output while requiring only one off-chip inductor, which yields many appealing advantages for mass-production and applications. A single-inductor dual-output (SIDO) boost converter is reported most recently in [1] and [2]. The SIDO converter works in pseudo-continuous or discontinuous conduction mode (PCCM/DCM) with a freewheel period, trying to handle large load currents and eliminate cross-regulation. However, PCCM operation unnecessarily dissipates energy in the resistance of the inductor and freewheel-switch because of the non-zero inductor current during the freewheel time, which reduces the overall efficiency. More disadvantageously, using separate proportional–integral (P-I) compensators and output-switch current sensors for the outputs with time-multiplexing control causes unwanted complexity and increases the chip area. Therefore, PCCM/DCM is not a good solution, especially when the number of outputs increases.

The SIMO converter described in this paper employs ordered power-distributive control (OPDC) to regulate four main positive boost outputs and one dependent negative output developed by a charge-pump. This converter can work in either DCM or CCM while maintaining low cross-regulation. Figure 29.9.1 shows the architecture of the 5-output SIMO DC-DC converter including important sub-blocks. The OPDC arranges four boost outputs V_{o1}, V_{o2}, V_{o3} and V_{o4} in descending order of priority to, one by one, share the charge from the inductor in every switching cycle. The first three output voltages V_{o1}, V_{o2} and V_{o3} are controlled using comparators and are, thus, called bang-bang outputs, while the last-ordered output V_{o4} is P-I controlled with an error amplifier responsible for the converter's total current. Therefore, in this OPDC, all of the errors of the preceding bang-bang outputs are transferred and accumulated to the last output, which is the only one requiring a compensation network in the feedback loop.

The operating principle of OPDC can best be explained using the timing diagram in Fig. 29.9.2. During the time denoted DT, the inductor current I_L ramps up at a rate of V_g/L. The duty-cycle D is determined by peak-current mode control. The 4 output switches S1, S2, S3, S4 and the freewheel switch Sf (which is active in DCM), in order, turn on during the time D′T, where D′ + D = 1. During D′T, I_L ramps down with different slopes depending on the output voltages and which output switches are on. S1 is on at the beginning of D′T, making I_L ramp down at a rate of $-(V_{o1} - V_g)/L$ and flow into V_{o1}. As soon as comparator CP1 detects that V_{o1} is larger than its target voltage, D_1T expires, S1 is turned off and S2 is turned on. The same sequence then repeats as the inductor current ramps down with a slope equal to $-(V_{o2} - V_g)/L$ during D_2T, then $-(V_{o3} - V_g)/L$ during D_3T, while V_{o2} and then V_{o3}, in turn, get the second and third portion of charge, respectively. Switch S4 is the last output switch to turn on and the last portion of charge flows into V_{o4} while the slope of the inductor current is $-(V_{o4} - V_g)/L$ during D_4T. When inductor current is zero, D_4T expires, S4 is off, and Sf turns on during D_fT to short the two ends of the inductor and suppress possible ringing at V_x until the end of the switching cycle. In this mode of operation, the converter is said to work in DCM. Since I_L does not decrease to zero in CCM operation, there is no freewheel period, which is indicated by D_fT in the figure, as illustrated by $I_L(1)$. Dependent on the last portion of charge, the loop containing V_{o4} and the total current loop are compensated and controlled by the well-known peak-current control method. These two control-loops guarantee that the last portion of charge be enough to keep channel 4 at its target voltage, while good voltage regulation is already maintained in the preceding outputs V_{o1}, V_{o2} and V_{o3}. The charge-pump circuit with two diodes and two capacitors at V_{oN} makes a negative output dependent on the voltage at V_x, where C_{N1} gets charge when V_x is high and transfers negative charged to C_{N2} when V_x goes low.

The stability and reliability of the converter are always obtained with both loops properly compensated. An accurate peak inductor-current sensor and a precise zero inductor-current sensor, partially reported in [3], are shown together in Fig. 29.9.3. The simplicity and flexibility of the OPDC prove that the converter can have different switching patterns in regulating the outputs. $I_L(2)$ illustrates CCM operation, where three or two output switches are alternately turned on in order during one switching cycle. Operation at the boundary of CCM and DCM and in DCM are illustrated by $I_L(3)$ and $I_L(4)$, respectively. OPDC allows the turn-on frequency of output switch to change depending on its duty D_i and load current. Voltage comparators, together with only one P-I voltage loop and one current-loop in OPDC, help maintain desirable low cross-regulation by recovering quickly from changes in the load as illustrated by $I_L(5)$ and $I_L(6)$.

In Fig. 29.9.1, the reference voltages are programmed by off-chip digital signals. A logic order control block passes the signals from comparators, in order of priority, to make OPDC. Dead-time logic guarantees appropriate non-overlap times between on-states of the power switches during transients and synchronous rectification is used for the four regulated outputs for high efficiency. Since V_{o1} is always the highest voltage, it biases all the bodies of the pMOS power transistors and supplies all gate drivers for the power transistors. The capacitor C_{N1} is chosen small enough not to affect the total operation and dead-time control.

The converter is implemented in 8.7mm^2 die area using a 0.5μm 1P3M BiCMOS process. It works for input voltages from 2.5 to 4.5V. The inductor is 10μH with a parasitic resistance of 350mΩ and the switching frequency is 700kHz. The four boost outputs V_{o1}, V_{o2}, V_{o3} and V_{o4} are programmable from 5 to 12V, but normally regulated at 10.2V, 7.0V, 7.5V and 8.0V, with ripple voltages of 85mV, 55mV, 55mV and 50mV, respectively. All four of these outputs use a 4.7μF/300mΩ-ESR filtering capacitor, satisfying line and load regulation standards for commercial products. The non-regulated dependent negative output V_{oN} is normally -9.5V and uses a 1μF filtering capacitor C_{N2}, a 1nF charge-pump capacitor C_{N1} and 0.35V Schottky diodes for high efficiency. Figures 29.9.4 and 29.9.5 show experiment results. Figure 29.9.4 shows the inductor current along with the waveform at V_x and AC-coupled output voltages V_{o1} and V_{o2}, in which V_{o2} is set to a lower voltage (5V) to see clear slope changes in the inductor current waveform at the boundary of CCM and DCM. Figure 29.9.5 shows CCM operation of the converter with normal output voltage settings. The experimental results agree well with OPDC operation as discussed above. Maximum output power is 850mW, and a maximum efficiency of 80.8% is achieved at a total output power of 450mW. The converter's performance is summarized in Fig. 29.9.6 and a die micrograph is shown in Fig. 29.9.7.

Acknowledgement:
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References:
[1]D. S. Ma, W. H. Ki and C. Y. Tsui, "A Pseudo-CCM/DCM SIMO Switching Converter With Freewheel Switching," *ISSCC Dig. Tech. Papers*, pp. 390-391, 2002.
[2] D. S. Ma, W. H. Ki and C. Y. Tsui, "A Pseudo-CCM/DCM SIMO Switching Converter With Freewheel Switching," *IEEE J. Solid-State Circuits*, pp. 1007-1014, June, 2003.
[3] Hanh-Phuc Le et al., "Integrated Zero-Inductor-Current Detection Circuit for Step-Up DC-DC Converters," *Electronics Letters*, Vol. 42, Issue 16, pp. 943-944, 2006.

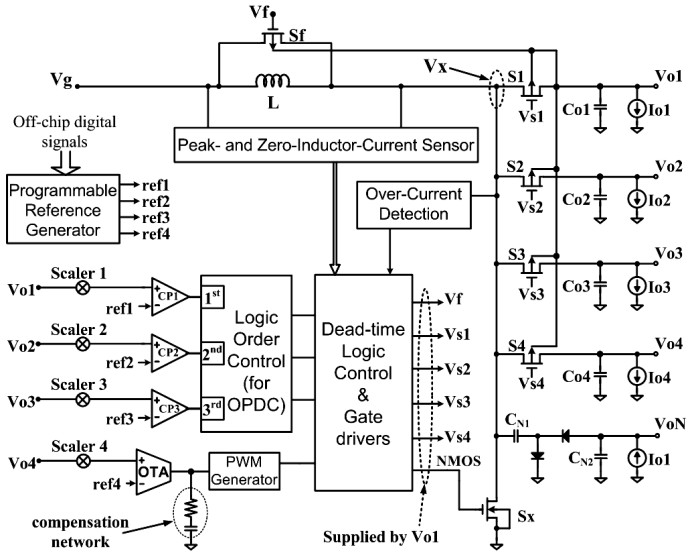

Figure 29.9.1: Architecture of the OPDC SIMO DC-DC converter.

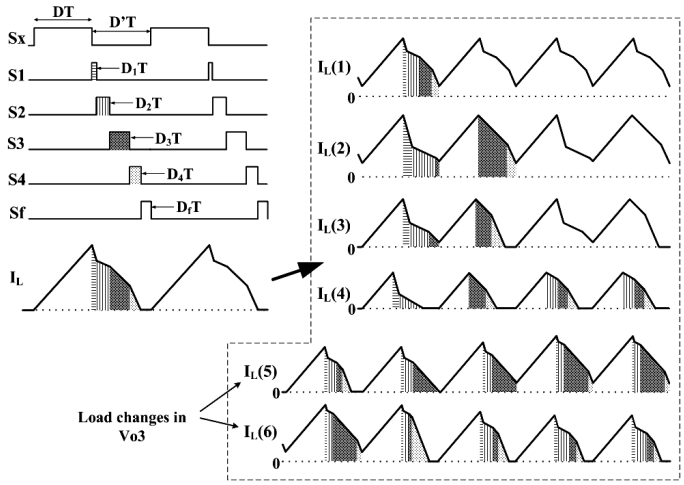

Figure 29.9.2: Timing diagram of the OPDC SIMO DC-DC converter.

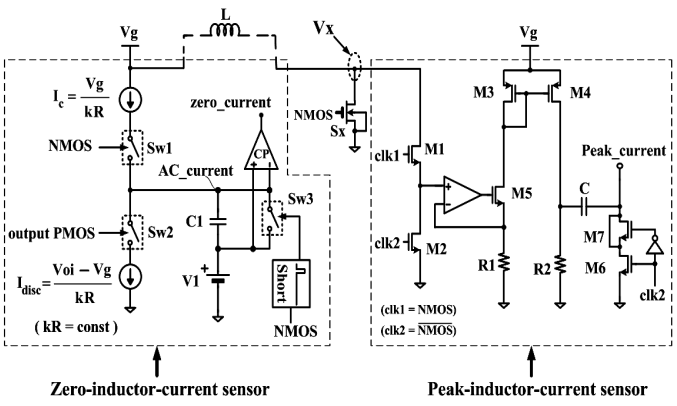

Figure 29.9.3: Peak inductor-current and zero inductor-current sensing circuits.

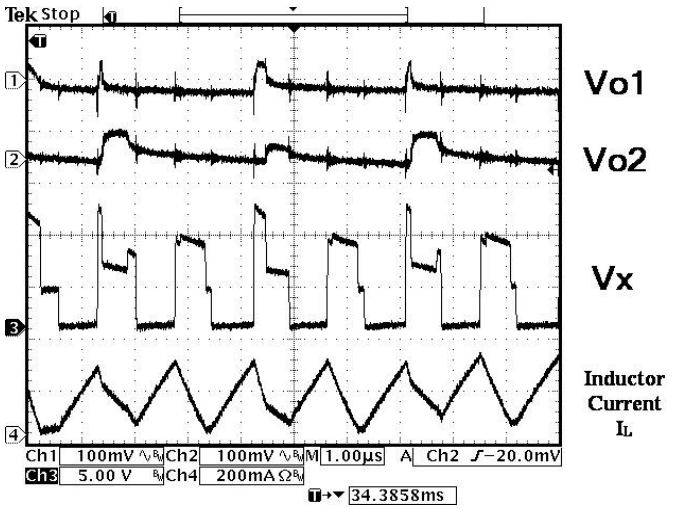

Figure 29.9.4: Measured waveforms at the boundary of DCM and CCM operation.

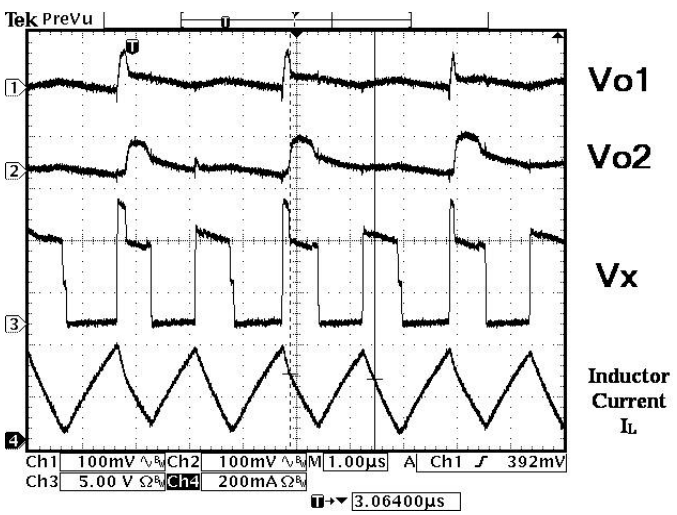

Figure 29.9.5: Measured waveforms in CCM operation.

Process	0.5µm Bi-CMOS, t-well, 3AL, 1PS				
Chip area	2.9 × 3.0mm²				
Package	QFN, 24 pins, 5 × 5mm²				
Supply voltage	2.5V to 4.5V (3.7V, nominal)				
Inductor/ESR	10µH / 350mΩ				
Oscillator frequency	700kHz (nominal)				
Current ripple	290mA				
Maximum efficiency	80.8 %				
Output	Vo1	Vo2	Vo3	Vo4	VoN
Voltage (V)	10.2	7.0	7.5	8.0	- 9.5
Load current (max) (mA)	5	30	30	40	5
Load regulation (mV/mA)	1.5	0.78	0.5	0.4	x
Line regulation (mV/V)	58	73	85	90	80
Output ripple (max) (mV)	160	140	140	120	60
Filtering capacitor / ESR (µF) / (mΩ)	4.7/300	4.7/300	4.7/300	4.7/300	1/250

Figure 29.9.6: Summary of the converter performance.

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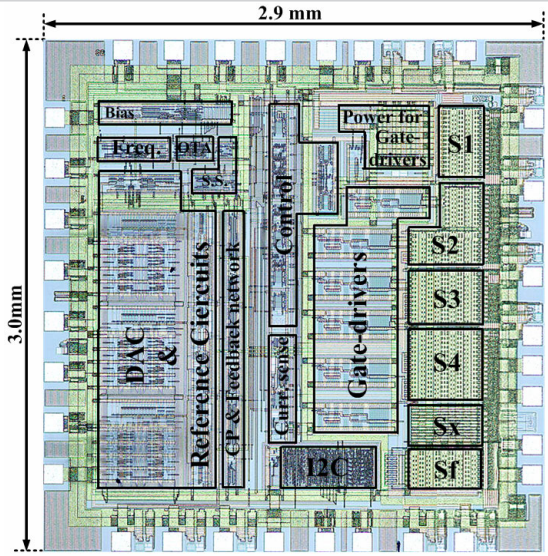

Figure 29.9.7: Die micrograph.

